Norwegian University of Science and Technology
Faculty of Information Technology, Mathematics and Electrical Engineering
The Department of Computer and Information Science

TDT4160
COMPUTER, FUNDAMENTALS
(DATAMASKINER GRUNNKURS)
EXAM

10. DECEMBER, 2008, 09:00–13:00

Contact:
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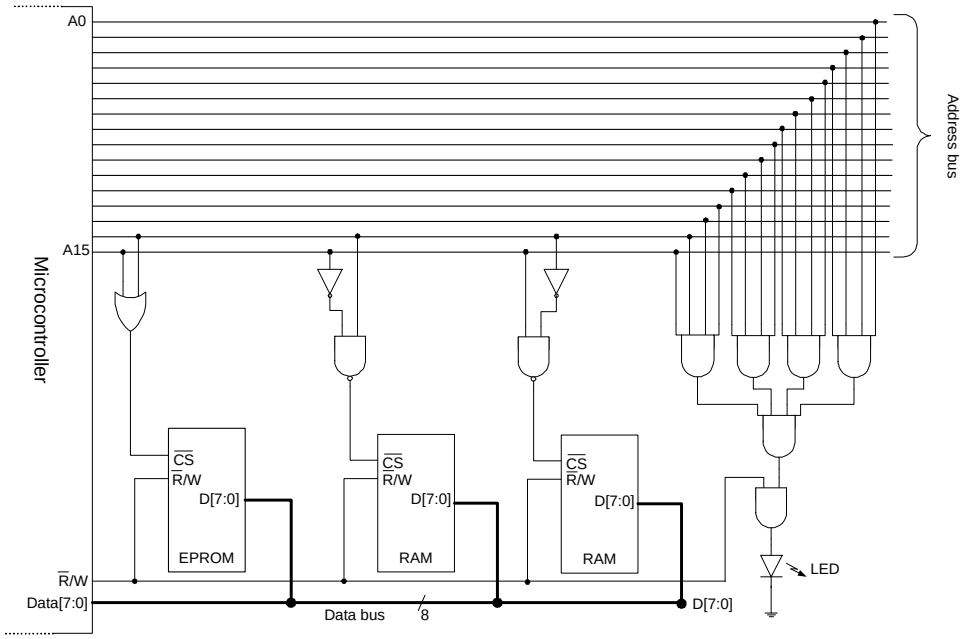
Examination support materials:
D.
No written and handwritten examination support materials are permitted.
A specified, simple calculator is permitted.

Language:
English

QUESTION 1: DIGITAL LOGIC LEVEL (20% (10% ON A, 5% ON B AND C))

a. In Figure 1 EPROM, RAM and a light emitting diode (LED) share a common bus. What are the memory address ranges for the devices? EPROM and RAM uses an active low (logic ”0”) Chip Select (CS) signal.



Figur 1: Address decoding.

b. Is it possible to extend the system with 16kB (16384 bytes) of RAM? Explain.

c. When is the LED lit?

QUESTION 2: MICROARCHITECTURE AND MICROINSTRUCTIONS (20% (5% ON A AND B; 10% ON C))

Use Figure 5, Figure 6, Figure 7 and Figure 8 for the IJVM in the appendix to answer the questions.

a. Explain the functionality of the register "MPC".

b. Create microinstruction(s) for the following IJVM operation: Load register "OPC" with the content of register "H".

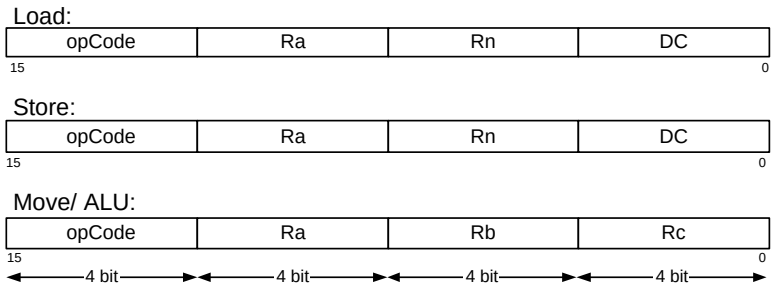
   You don't need to consider the Addr and J fields. Give the correct bit value for the ALU, C, Mem and B fields —see Figure 6.

c. Create microinstruction(s) for the following IJVM operation:
   TOS = LV + (OPC + 1).

   You don't need to consider the Addr and J fields. Give the correct bit value for the ALU, C, Mem and B fields —see Figure 6.

QUESTION 3: INSTRUCTION SET ARCHITECTURE LEVEL (ISA)(20%)

In an imaginary 16 bit architecture there exists only three types of instructions: Load, Store and MOVE/ALU. Figure 2 shows the format of the three instruction types.



Load:
- Ra: points to memory location, any user register
- Rn: data destination register, any user register
- DC: Don't Care, not in use

Store:
- Ra: points to memory location, any user register
- Rn: data source register, any user register
- DC: Don't Care, not in use

Move/ ALU::
- Ra: destination register, any user register
- Rb: source register, any user register
- Rc: source register, any user register

Figur 2: Possible instruction types.

a. From the available information:

   i) What is the maximum number of instructions possible? Explain.

   ii) What is the maximum number of user registers this machine can have? Explain.

b. What type of architecture is this instruction set for?

c. If the format is changed for the load/store to a format using the DC field as an index for a base address in *Ra,* the addressing mode is changed. Does this change have any influence on the ISA definition for the machine? Explain.

d. The shown machine is most likely a RISC machine. Why?

QUESTION 4: COMPUTERS (20% (8% ON A AND C; 4% ON B))

a. Figure 9 and Figure 10 in the appendix shows different versions of the IJVM microarchitecture. What features are introduced and how does such features influence on the performance compared to the original microarchitecture shown in Figure 5?

b. What implications do the changes in microarchitecture in question "a" have on the ISA level?

c. See Figure 5, Figure 8 and Figure 10. Approximately, what can the clock period be reduced to if the microarchitecture is changed from the implementation shown in Figure 5 to the implementation shown in Figure 10?

QUESTION 5: MISCELLANEOUS (20%)

Pick the right answer in the following questions. Correct answer gives 4% score, wrong answer gives -2% and don't know (no answer, more then one answer) gives 0% score.

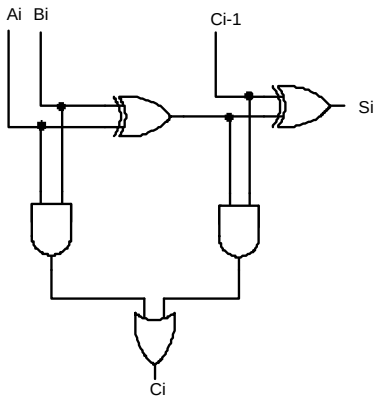
a. What is stored in the *Addr* field of *MIR*? See Figure 5.

   1) The Address of the next microinstruction in *control store*.
   2) Contains only a valid address if a conditional branch is to be executed, activation of the J bit.
   3) At all time a copy of the content of *MBR*.
   4) *control store* start and end address for the active microinstruction.

b. What claim is correct for a Chip Multi Processor (CMP)?

   1) Is an Array computer.
   2) Is of type SIMD.
   3) Is of type homogeneous or heterogeneous.
   4) Is a MIMD type that always uses a crossbar for communication between the processor cores.

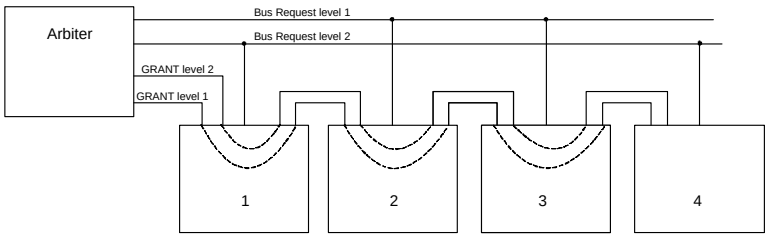
c. What is illustrated in Figur 3?



Figur 3: Mysterious device.

1) Full adder.
2) Half adder.
3) Static RAM cell.
4) Multiplexer.

d. What is the order of priority for the devices in Figure 4. Level 1 has higher priority then level 2. The priority is ordered from high to low.



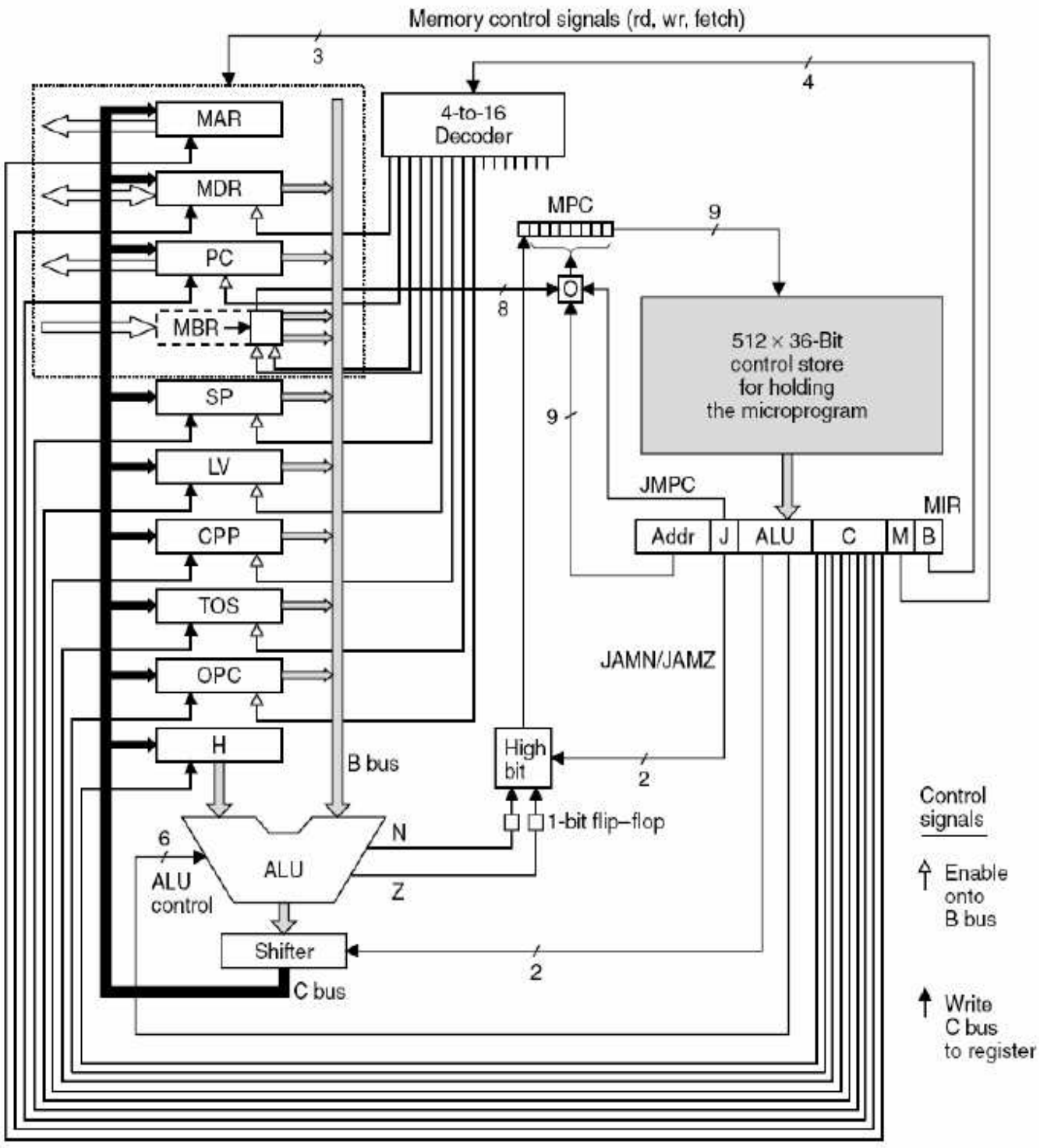
Figur 4: Centralized bus arbiter.

1) 1, 2, 3, 4.
2) 2, 3, 1, 4.
3) 1, 4, 2, 3.
4) 3, 2, 4, 1.

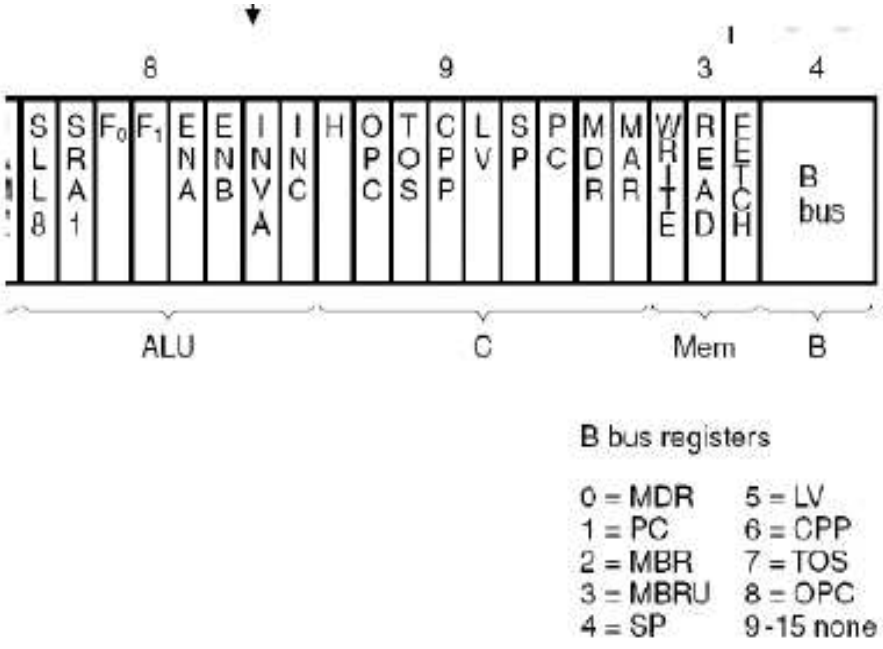
e. Which of the following claims regarding computer components is correct?

1) Asynchronous bus transfer must use a global clock.
2) An ALU that can perform addition and invert can also subtract.
3) EPROM and flash memory are functional equivalent.
4) EEPROM and flash memory are functional equivalent

IJVM appendix



Figur 5: Block diagram (IJVM).

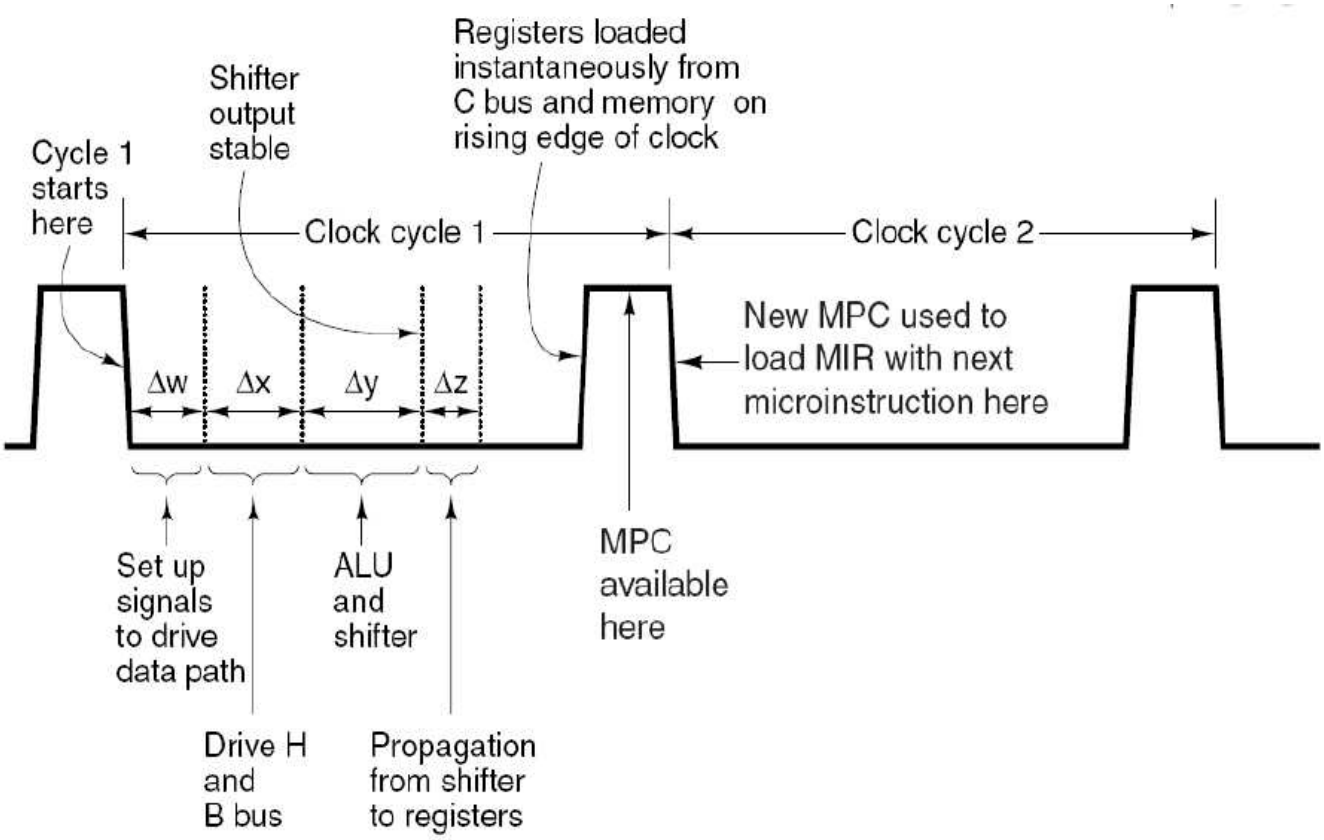


Figur 6: Microinstruction format (IJVM).

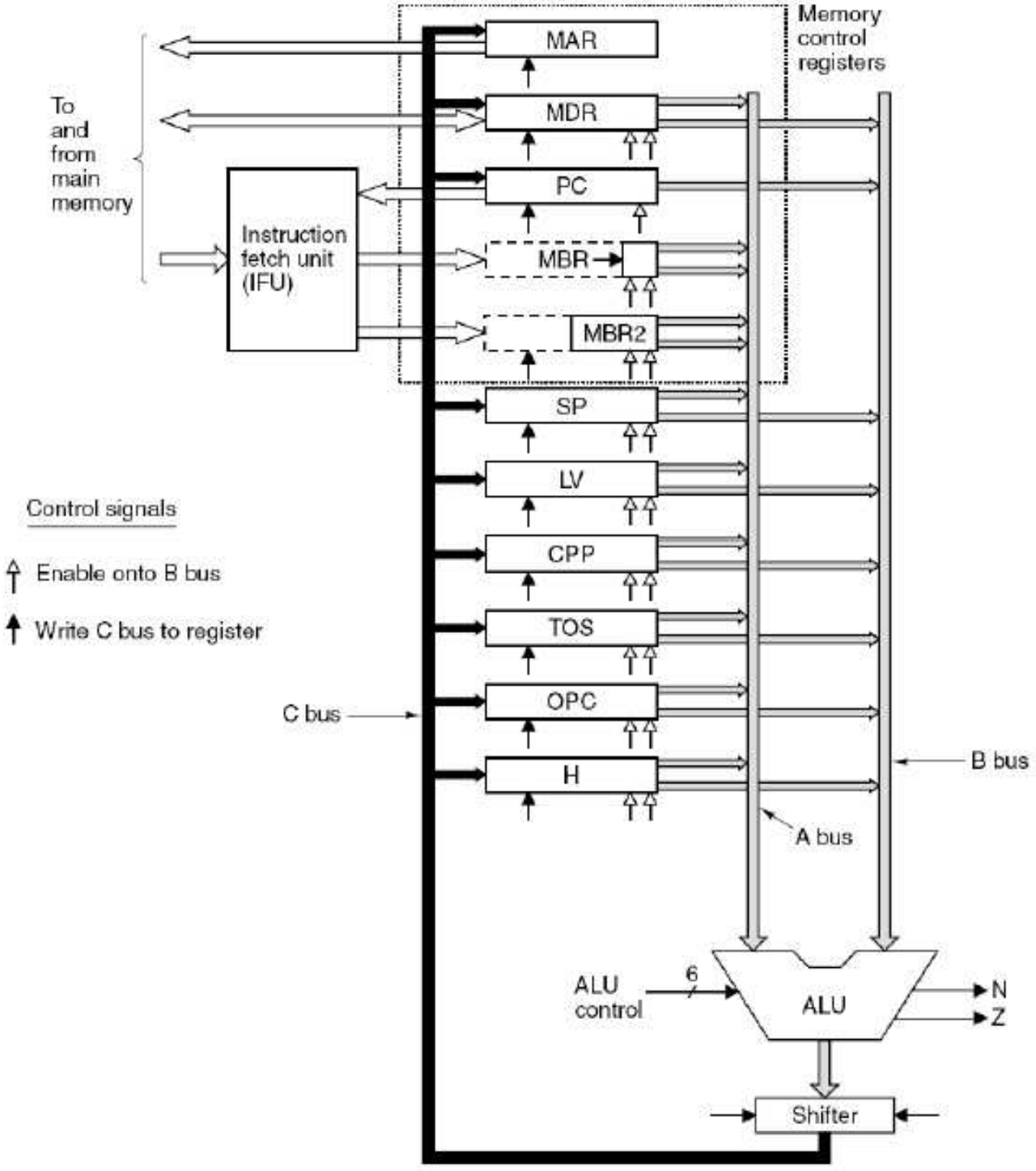
F_0	F_1	ENA	ENB	$\overline{\text{INVA}}$	INC	Function
0	1	1	0	0	0	A
0	1	0	1	0	0	B
0	1	1	0	1	0	$\overline{A}$
1	0	1	1	0	0	$\overline{B}$
1	1	1	1	0	0	A + B
1	1	1	1	0	1	A + B + 1
1	1	1	0	0	1	A + 1
1	1	0	1	0	1	B + 1
1	1	1	1	1	1	B – A
1	1	0	1	1	0	B – 1
1	1	1	0	1	1	–A
0	0	1	1	0	0	A AND B
0	1	1	1	0	0	A OR B
0	1	0	0	0	0	0
1	1	0	0	0	1	1
1	1	0	0	1	0	–1

SLR1	SLL8	Function
0	0	No shift
0	1	Shift 8 bit left
1	0	Shift 1 bit right

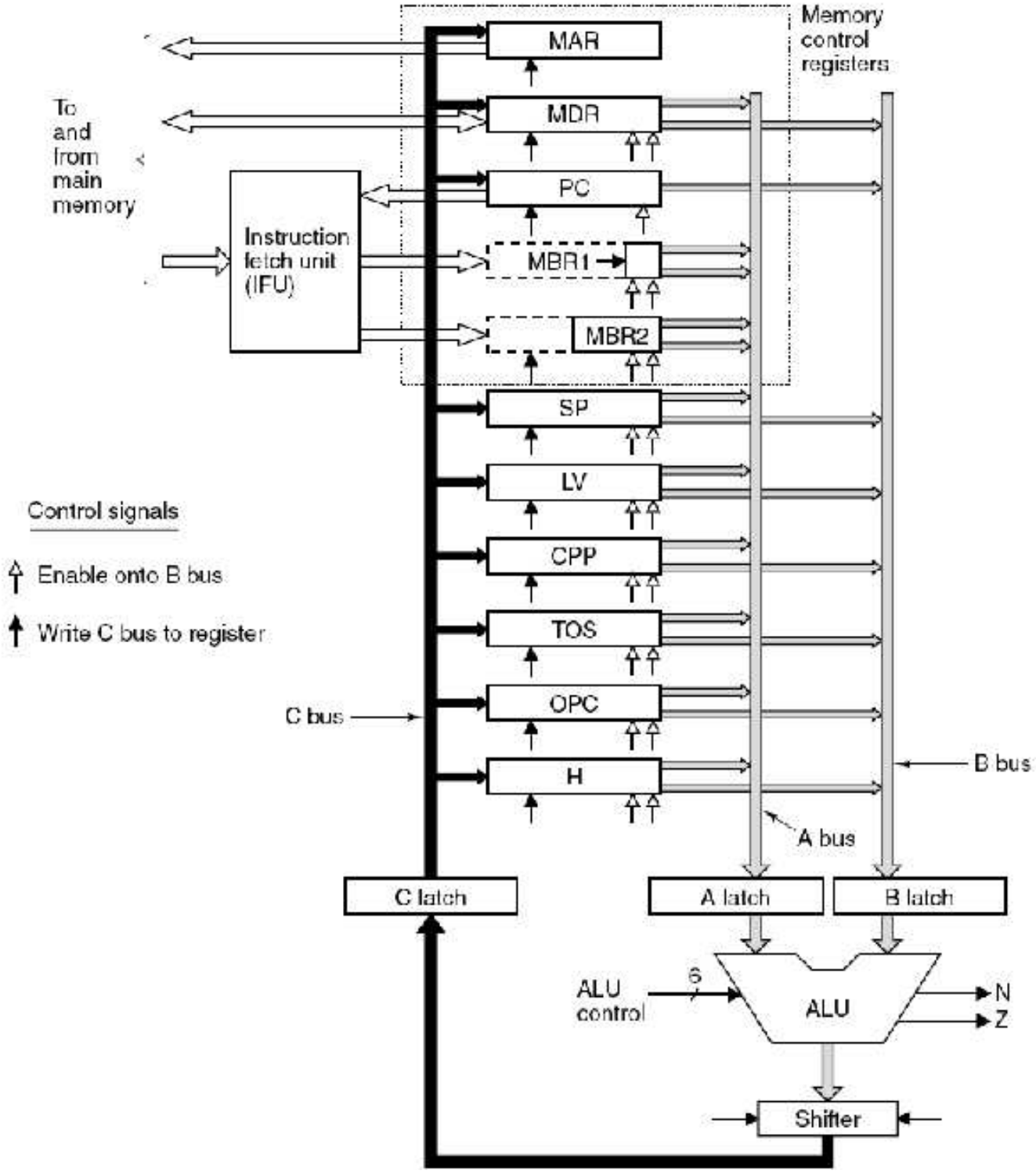
Figur 7: ALU functions (IJVM).



Figur 8: Timing diagram (IJVM).



Figur 9: Alternative microarchitecture I.



Figur 10: Alternative microarchitecture II.