Norwegian University of Science and Technology

DEPARTMENT OF COMPUTER AND INFORMATION SCIENCE

MID-TERM EXAM
TDT4258 MICROCONTROLLER SYSTEM DESIGN

Wednesday 3th Mars 2010

Time: 1615 - 1745

Allowed material: D: No printed or handwritten material allowed
Specific, simple calculator allowed

Use the table provided on the final sheet to provide your answers

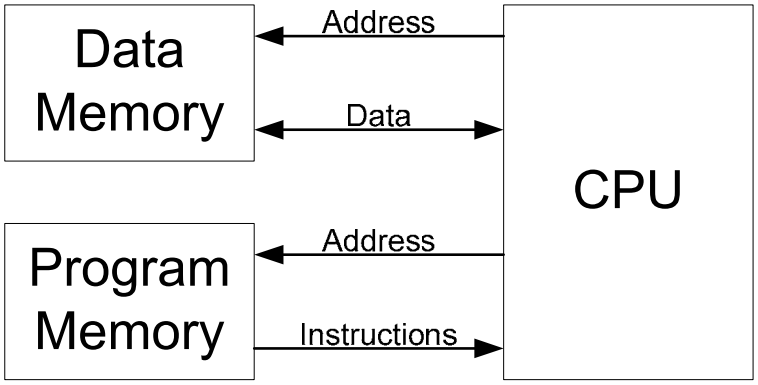
Set type English E

Correct answer: 2.5 points
Wrong answer: -0,5 points
Unanswered: 0 points
Multiple answers on one question: -0,5 points!

The mid-term yields a maximum of 20 points, which are then recalculated to account for 20% of the final grade.

ANSWERS ARE TO BE SUBMITTED ON A SEPARATE SHEET ATTACHED AS THE FINAL PAGE

a) Given the information in the figure, what statement is correct?



A1. The figure shows a computer with a typical *accumulator architecture*
A2. The figure shows *a von Neumann architecture computer*
A3. The figure shows *a Harvard architecture computer*
A4. From the information in the figure, a RISC implementation can be excluded
A5. From the information in the figure, a CISC implementation can be excluded

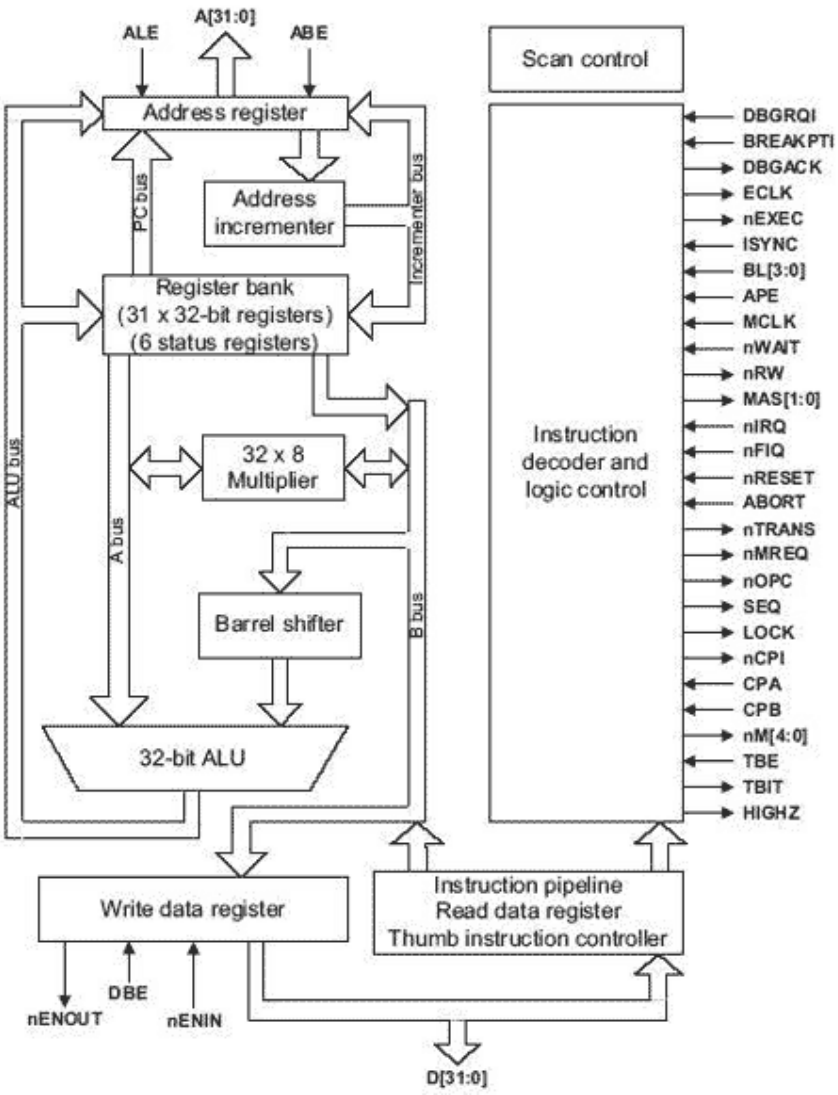
b) At what level in the design process is a block diagram a suitable abstraction level?

B1. R*equirements*
B2. S*pecification*
B3. A*rchitecture*
B4. C*omponents*
B5. S*ystem integration*

c) What claim regarding interrupts is **not** correct??

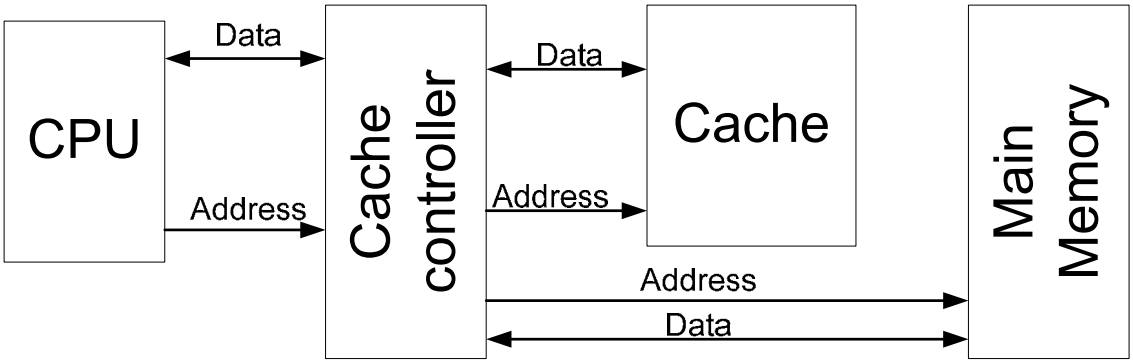
C1. NMI is an interrupt used by units that include *non-volatile memory*
C2. NMI is an interrupt at the highest level that can not be masked by users
C3. In the *interrupt priority register* the user can specify what I/O unit that should have the highest priority if several I/O units signal an interrupt at the same time
C4. The *interrupt register* indicates what source that requested an interrupt
C5. Using interrupts instead of busy wait free CPU time

d) In the figure some of the internal architecture of an ARM processor is shown. Use the figure to find what claim that is **not** correct (alternatively that statement D5 is correct)?



D1. It is possible to do an addition of two registers and write the result back to one of the two registers in one operation, e.g. R0 = R0 + R3
D2. It is possible to do an ALU operation between two registers and write the result back to a third register in one operation, e.g. R0 = R2 + R3
D3. The processor supports multiplication
D4. It is possible to do instructions that supports shift in combination with ALU operations, e.g. R0 = R2 + (R3 << 1)
D5. All the above statements are correct

e) Given a system, shown in the figure, with a 16-bit microcontroller with 8 general 16-bit registers, 16-bit fixed instruction size, 128KB of cache 16MB of off-chip DRAM, which one of the following statements is **not** correct (alternatively that statement E5 is correct)?



E1. In this system, memory access time will be non-deterministic compared to a system with no cache

E2. Average memory access time (tav) will be: $tav = h*t_{cache} + (1-h)*t_{main}$

h: cache hit rate

t_{cach}: cache access time

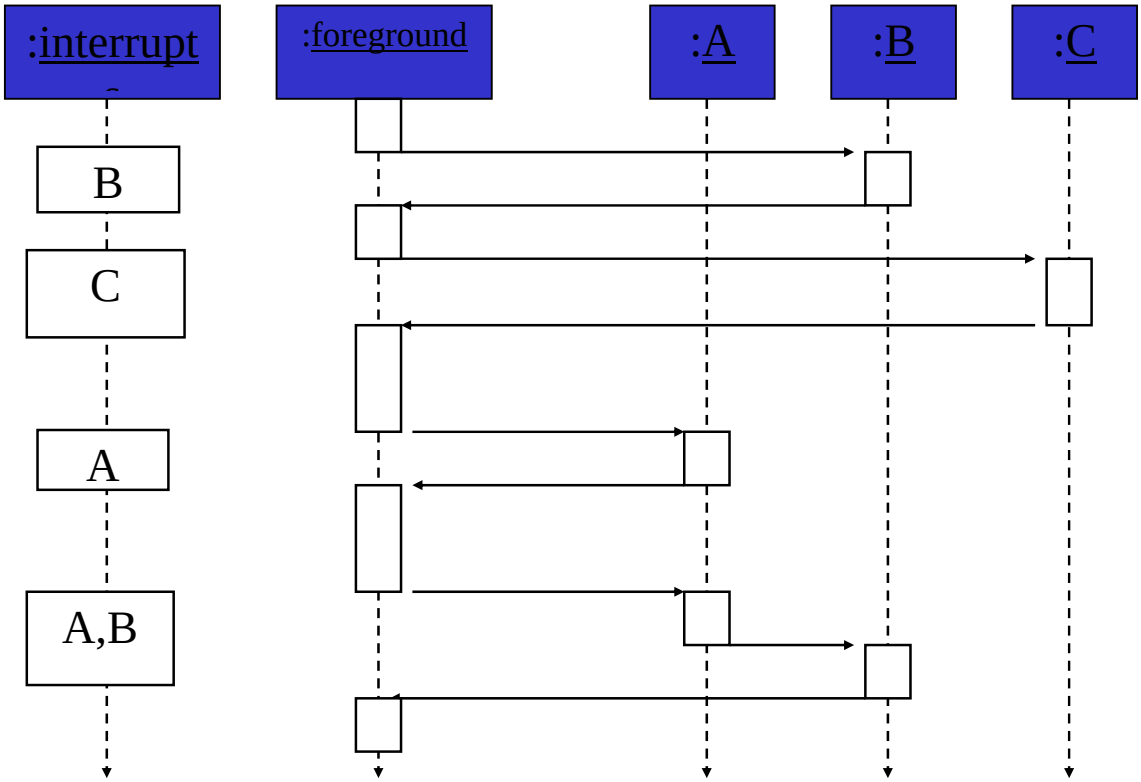
t_{main}: main memory access time

E3. This system only include *L1 cache*

E4. All memory access is done by the cache controller

E5. All the above statements are correct

f) The figure shows how a processor alternate between executing instruction in a program (foreground) and executing instructions in interrupt routines for three I/O units (A, B and C). From the information in the figure, how are the interrupts prioritized?



F1. All interrupts has equal priority
F2. A has higher priority then B
F3. C highest, thereafter B and A lowest
F4. B highest, thereafter A and C lowest
F5. B has higher priority then A

g) Hvilken påstand om prosesser er **ikke** riktig?

G1. Kontekstbyttefrekvens kan påvirke hurtigbufferutnyttelse
G2. En prosess som etterspør data som må hentes fra hovedlager (eng: *main memory*) vil av scheduleren vanligvis settes i en ventende tilstand (eng: *waiting*).
G3. Semaforer kan alltid implementeres i et program ved å utføre to etterfølgende instruksjoner, en som tester en verdi, og en som setter verdien basert på foregående test.
G4. POSIX støtter valg av scheduleringsmetode for hver enkelt prosess
G5. Co-operative multitasking er sårbart med tanke på prosesser som "henger" (slutter å respondere)

h) Hvilken påstand om nettverk og kommunikasjon er **ikke** riktig?

H1. OSI-modellen abstraherer nettverkskommunikasjon med en 7-lags modell
H2. I^2C-bussen benytter to linjer, SDL (serial data line) og SCL (serial clock line)
H3. En I^2C-buss kan ha flere mastere

H4. En I^2C-overføring inkluderer et CRC-felt for feildeteksjon
H5. En CAN-buss kan benytte et tvunnet par som sitt overføringsmedium

Studentnummer:

Studieprogram:

Answering table:

Mark with a cross the box that gives the correct answer for each question. Be warned that the **answers are NOT provided in order**. Double check that your crosses provide the intended answers.

a)	A1	A3	A2	A4	A5
b)	B5	B1	B3	B2	B4
c)	C4	C5	C1	C3	C2
d)	D2	D4	D5	D1	D3
e)	E3	E2	E4	E5	E1
f)	F1	F3	F2	F4	F5
g)	G5	G1	G3	G2	G4
h)	H4	H5	H1	H3	H2

Deliver only this answer table
Keep the questionare

REMEMBER TO WRITE BOTH YOUR STUDENT ID NUMBER AND PROGRAM OF STUDY

DO NOT TURN BEFORE BEING ALLOWED TO DO SO !