Norwegian University of Science and Technology
Department of Computer and Information Science

Contact:
Magnus Jahre (952 22 309)

TDT4258 MICROCONTROLLER SYSTEM DESIGN TEST

Tuesday 12. April
Time: 12:30 – 14:00
ENGLISH

Allowed Aids:
D.
No written or handwritten examination support materials are permitted.
A specified, simple calculator is permitted.

Use the provided space to answer the problems. If you need more space, an extra answer box is available on the last page of the test. The test accounts for 40% of the final grade, and the provided points show the maximal number of points that can be achieved on each assignment. Read the problem texts throughly.

Student Number:

Problem 1 Multiple Choice (20 points)

Answer by circling the answer alternative you believe is the correct answer. You are awarded 2.5 points for a correct answer and 0 points if you do not answer. If your answer is wrong or you circle more than one alternative, you will get -1 points.

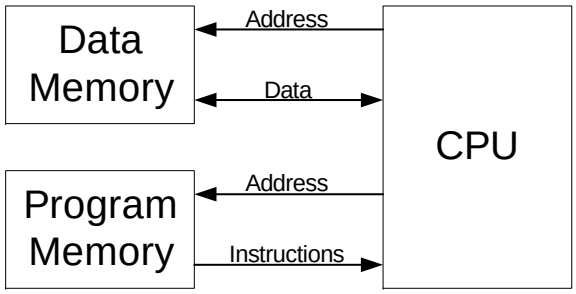

Figure 1: High-Level Architecture

a) (2.5 p) Which of the below statements is correct given the high-level system architecture in Figure 1?

1. The figure shows a typical accumulator architecture
2. The figure shows a typical Von Neumann architecture
3. The figure shows a typical Harvard architecture
4. The figure shows a typical Bauhaus architecture

Riktig svar: Alternativ 3

b) (2.5 p) In which stage of a design process is a block diagram a good level of abstraction?

1. Requirements
2. Specification
3. Architecture
4. System Integration

Riktig svar: Alternativ 3

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c) (2.5 p) If a microcontroller has memory mapped I/O, it means that:

1. Each I/O controller has a set of registers and each register is mapped on a specific address in the processor's address space
2. Device specific instructions are used to read and to write to I/O devices
3. Each I/O device is represented as a file in the /dev folder
4. CPU saves the state of its parts and jumps to an interrupt routine whenever a signal from an I/O device is received

Riktig svar: Alternativ 1

d) (2.5 p) A device driver is:

1. A software layer between the application and the actual device that provides a well defined programming interface and hides the technical details of how the device works
2. An application that runs in the user space and uses specific built-in kernel system calls to control the I/O devices
3. A special file in the /dev folder that is represented by a major and minor number, uniquely identifying a specific I/O device
4. A device that is used to combine several interrupt sources onto one CPU pin

Riktig svar: Alternativ 1

e) (2.5 p) Which of the following statements about memory management is *not* correct?

1. The virtual to physical address translation is commonly carried out by the Memory Management Unit (MMU)
2. Paged memory management uses fixed size memory blocks
3. A Translation Lookaside Buffer (TLB) can be used with both paged and segmented memory management
4. Segmented memory management suffer from internal fragmentation

Riktig svar: Alternativ 4

Student Number:

f) (2.5 p) Which of the following statements about I/O is *not* correct?

1. Polling and Busy-Wait I/O are different names for the same technique
2. When an interrupt is handled, it is necessary to save all CPU state
3. Interrupt priorities are orthogonal to interrupt vectors
4. A vectorized interrupt is implemented by storing a pointer to a handler function in an interrupt vector table

Riktig svar: Alternativ 2

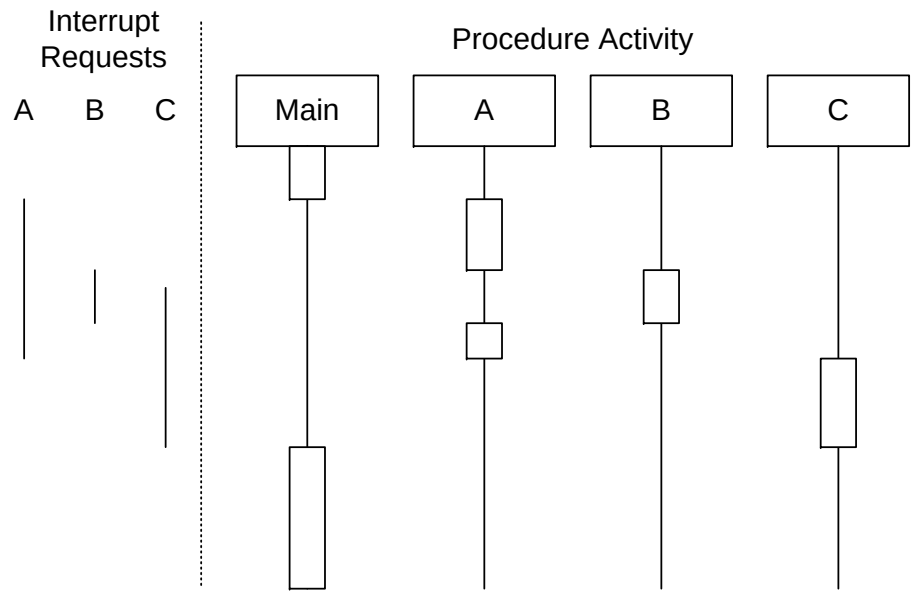

Figure 2: Interrupt Sequence Diagram

g) (2.5 p) Which of the statements below are *not* correct given the information in Figure 2?

1. A has a higher priority than B
2. B has a higher priority than C
3. C has a lower priority than A
4. C has a lower priority than B

Riktig svar: Alternativ 1

h) (2.5 p) Which statement regarding multitasking is *not* correct?

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1. Cooperative multitasking depends on the process actively yielding the CPU
2. Cooperative multitasking cannot support process priorities
3. Preemptive multitasking cannot be implemented without interrupts
4. Preemptive multitasking is more robust to programming errors than cooperative multitasking

Riktig svar: Alternativ 2

Student Number:

Problem 2 Program Optimization (10 points)

```
#define INDEX(i,j,n) ((n*i)+j)

void copy(int* x, int* y, int A){
  int i=0;
  int j=0;
  for(i=0;i<A;i++){
    for(j=0;j<A;j++){
      if(j > 0){
        x[INDEX(i,j,A)] = y[INDEX(i,j,A)];
      }
      else{
        x[INDEX(i,j,A)] = 0;
      }
    }
  }
}
```

a) (5 p) Draw the control-dataflow graph (CDFG) for the procedure *copy*.

Løsning: The CDFG is in Figure 3

b) (5 p) Optimize the procedure *copy* with the technique *Induction Variable Elimination*.

Løsning:

```
void copy(int* x, int* y, int A){
int i=0;
for(i=0;i<A*A;i++){
if(i%A != 0) x[i] = y[i];
else x[i] = 0;
}
}
```

Problem 3 Processor-Based Systems (10 points)

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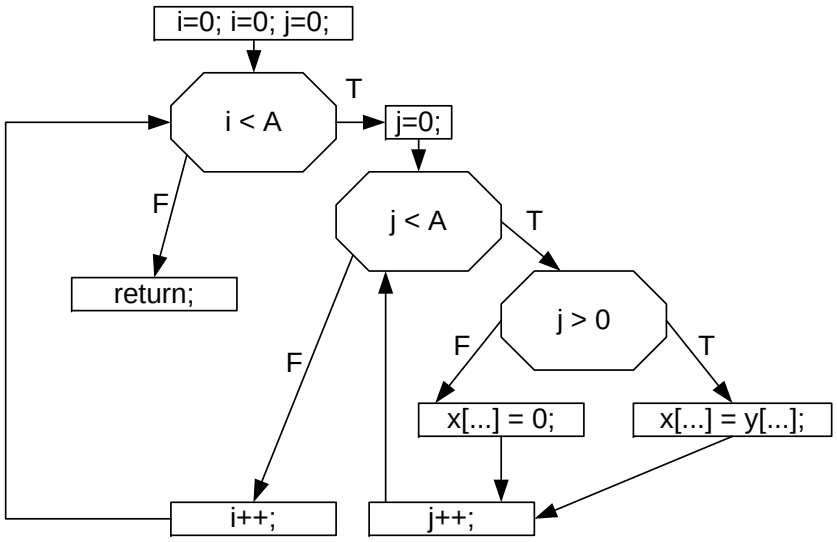

Figure 3: CDFG

a) (5 p) Draw a state machine describing the operation of a DRAM main memory.

Løsning: See slides from lecture 6, slide 8

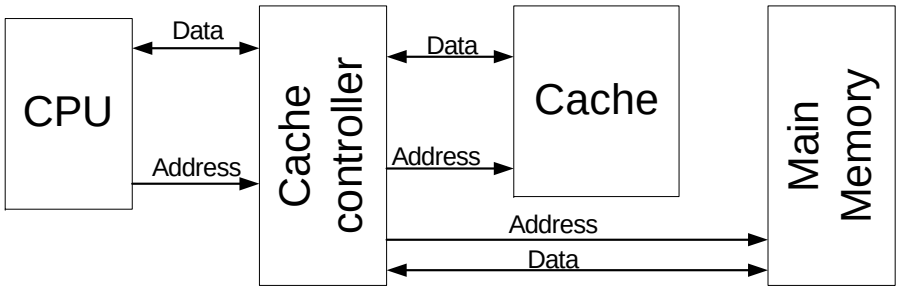

Figure 4: CPU with Memory System

b) (5 p) Figure 4 shows a high level block diagram of a processor-based system. The cache controller overhead is 1 clock cycle, the cache access time is 2 clock cycles and the main memory access time is 100 clock cycles. If we assume a cache hit rate of 90%, what is the lowest possible average memory access time for the CPU?

Løsning: Main observation: To achieve the lowest possible latency, the cache controller should access the main memory and cache in parallel.

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For 90% of the requests, the latency is the controller overhead plus the cache access time: $1 + 2 = 3$ clock cycles.
For 10% of the requests, the latency is the controller overhead plus the memory access time: $1 + 100 = 101$ clock cycles.

This gives an average memory access time of $0.9 \cdot 3 + 0.1 \cdot 101 = 12.8$ clock cycles.

Student Number:

Additional Answer Space

Student Number:

—OOO—

Do not turn over until instructed to do so!

Student Number: